In the Claims

Please amend the claims in the manner indicated below.

1. (currently amended) A method of forming a semiconductor device comprising:

forming a first patterned conductive layer on a dielectric material on a substrate;

forming a non-organic first barrier layer on a ~~the~~ surface of the first patterned conductive layer;

forming a second barrier layer of silicon carbide on a ~~the~~ surface of the first barrier layer;

forming a dielectric layer on a ~~the~~ surface of the second barrier layer; and

forming one of a via and a trench through a first portion of the dielectric layer and through a first portion of one of the first and second barrier layers;

wherein the first and second barrier layers are to prevent diffusion of metal from the first patterned conductive layer into the dielectric layer.

~~wherein the via is filled with a sacrificial light absorbing material.~~

2. (cancelled)

3. (previously amended) The method of claim 1 further comprising forming the trench through a second portion of the dielectric layer if the via is formed through the first portion of the dielectric layer.

4. (currently amended) The method of claim 1, wherein said one of the via and the trench is filled with a ~~the~~ sacrificial light absorbing material ~~comprises at least one of a dyed spin-on polymer and a dyed spin-on glass with dry etch properties similar to the dielectric layer~~.

5. (previously amended) The method of claim 1 further comprising forming the via through a second portion of the dielectric layer if the trench is formed through the first portion of the dielectric layer.

6. (previously amended) The method of claim 1 further comprising forming said one of the via and the trench through the second barrier layer followed by forming said one of the via and the trench through the first barrier layer.

7. (previously amended) The method of claim 6 wherein said one of the via and the trench is formed through the first and the second barrier layer with a single etch pass.

8. (currently amended) The method of claim 1 wherein the first barrier layer comprises a thickness of less than 20 nanometers of silicon nitride.

9. (currently amended) The method of claim 8 wherein the first barrier layer comprises a thickness of between 1 nanometer and 7 nanometers of silicon nitride.

10. (currently amended) The method of claim 1 wherein the second barrier layer comprises a thickness of less than 200 nanometers ~~of silicon carbide~~.

11. (currently amended) The method of claim 8 wherein the silicon nitride is deposited using any ~~one~~ of a plasma enhanced chemical vapor deposition process, a chemical vapor deposition process and an atomic layer deposition process.

12. (currently amended) The method of claim 10 wherein the silicon carbide is deposited using any ~~one~~ of a plasma enhanced chemical vapor deposition process, a chemical vapor deposition process and an atomic layer deposition process.

13. (currently amended) A method of forming a semiconductor device comprising:

forming a first patterned conductive layer on a dielectric material on a substrate;

forming a first barrier layer comprising silicon nitride on the surface of the first patterned conductive layer;

forming a second barrier layer comprising silicon carbide on the surface of the first barrier layer;

forming a dielectric layer on the surface of the second barrier layer; and

forming, through a first portion of the dielectric layer, either of a via and a trench ~~filled with a sacrificial light absorbing material;~~ .

14. (cancelled)

15. (previously amended) The method of claim 13 further comprising forming the trench through a second portion of the dielectric layer if the via is formed through the first portion of the dielectric layer.

16. (currently amended) The method of claim 13, wherein <u>said either of the via and the trench is filled with a</u> ~~the~~ sacrificial light absorbing material <u>comprising</u> ~~comprises~~ at least one of a dyed spin-on polymer and a dyed spin-on glass with dry etch properties similar to the dielectric layer.

17. (previously amended) The method of claim 13 further comprising forming the via through a second portion of the dielectric layer if the trench is formed through the first portion of the dielectric layer.

18. (original) The method of claim 13 wherein said either of the via and the trench is formed through the first and the second barrier layer with a single etch pass.

19. (currently amended) The method of claim 13 wherein the first barrier layer comprises a thickness of between 1 nanometer and 7 nanometer of silicon nitride.

20. (currently amended) The method of claim 13 wherein the second barrier layer comprises a thickness of less than 200 nanometers of silicon carbide.

21. (currently amended) The method of claim 13 wherein at least one of the silicon nitride and the silicon carbide is deposited using any one of a plasma enhanced chemical vapor deposition process, a chemical vapor deposition process and an atomic layer deposition process.

22. (currently amended) A method of forming a semiconductor device comprising:

forming a first patterned conductive layer on a dielectric material on a substrate;

forming a first barrier layer comprising silicon nitride on the surface of the first patterned conductive layer;

forming a second barrier layer comprising silicon carbide on the surface of the first barrier layer;

forming a dielectric layer on the surface of the second barrier layer; and

forming a via filled with sacrificial light absorbing material through a first portion of the dielectric layer and through a first portion of one of the first and second barrier layers.

23. (original) The method of claim 22 further comprising forming any one of a via, and a trench through a first portion of the dielectric layer.

24. (original) The method of claim 23 further comprising forming a trench through a second portion of the dielectric layer if the via is formed through the first portion of the dielectric layer.

25. (previously amended) The method of claim 24, wherein the sacrificial light absorbing material comprises at least one of a dyed spin-on polymer and a dyed spin-on glass with dry etch properties similar to the dielectric layer.

26. (original) The method of claim 24 further comprising forming a via through a second portion of the dielectric layer if the trench is formed through the first portion of the dielectric layer.

27. (original) The method of claim 24 further comprising forming the via through the second barrier layer followed by forming the via through the first barrier layer.

28. (original) The method of claim 27 wherein the via is formed through the first and the second barrier layer with a single etch pass.

29. (currently amended) The method of claim 22 wherein the first barrier layer comprises a thickness of between 1 nanometer and 7 nanometer of silicon nitride.

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30. (currently amended) The method of claim 22 wherein the second barrier layer comprises a thickness of less than 200 nanometers of silicon carbide.